In re Patent Application of:
ROCHE ET AL.
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In the Claims:

Claims 1-19 (Cancelled).

20.　(Previously Presented) A method of transmitting data between two devices via a clock line and at least one data line, the clock line being maintained by default on a first logic value, the method comprising:

providing each device with the ability to tie the clock line to a potential representing a second logic value opposite the first logic value;

tying the clock line to the second logic value, via the two devices, after data is applied to the data line;

maintaining the tie to the clock line by the device to which the data is sent while the device has not read the data; and

maintaining the data on the data line by the device sending the data at least until an instant when the clock line is released by the device to which the data is sent.

21.　(Previously presented) A method according to Claim 20, wherein one of the two devices is a master device and the other is a slave device, the master device tying the clock line to the second logic value before the slave device when data is transmitted, regardless of the direction in which the data is transmitted.

22.　(Previously presented) A method according to Claim 21, wherein the master device ties the clock line to the second

logic value after applying data to the data line when the master
device is sending the data to the slave device.

23.   (Previously presented) A method according to Claim
22, wherein the slave device detects the second logic value on
the clock line, then ties the clock line to the second logic
value and reads the data, when the slave device is receiving the
data from the master device.

24.   (Previously presented) A method according to Claim
23, wherein a time period that the slave device has to release
the clock line after receiving data, is independent of any action
by the master device, as the master device does not send any new
data while the slave device has not released the clock line.

25.   (Previously presented) A method according to Claim
21, wherein the master device ties the clock line to the second
logic value when the master receives data from the slave device.

26.   (Previously presented) A method according to Claim
25, wherein the slave device detects the second logic value on
the clock line, then ties the clock line to the second logic
value, and applies the data to the data line, when the slave
device is sending data to the master device.

27.   (Previously presented) A method according to Claim
26, wherein a time period that the slave device has to release
the clock line after sending the data, is independent of any

action by the master device, as the master device does not tie
the clock line to the second logic value to request a new data
until the slave device has released the clock line.

28.   (Previously presented) A method according to Claim
21, wherein when the clock line has the first logic value, a time
period that the master device has to tie the clock line to the
second logic value is independent of any action by the slave
device.

29.   (Currently Amended) A method according to Claim
21, further comprising providing the slave device with a
communication interface circuit including:
        a trigger ~~means~~ for automatically tying the clock line
to the second logic value when the clock line is changing from
the first logic value to the second logic value;
        an input for applying a clock line release signal to
the trigger ~~means~~; and
        an output for delivering a status signal that has a
first value when the clock line is tied to the second logic value
by the trigger ~~means~~ and a second value when the clock line is
released by the trigger ~~means~~.

30.   (Currently Amended) A method according to Claim
29, wherein the communication interface circuit further
comprises:
        storage ~~means~~ for storing at least one data; and
        an applicator ~~means~~ for automatically applying the at

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least one stored data to the data line when the clock line
changes from the first logic value to the second logic value.

31.   (Previously presented) A method according to Claim
20, wherein the first logic value is 1 and the second logic value
is 0.

32.   (Previously Presented) A method of transmitting
data between two devices connected via a clock line and at least
one data line, the method comprising:
        maintaining the clock line on a first logic value as a
default;
        providing each device with the ability to tie the clock
line to a potential representing a second logic value;
        tying the clock line to the second logic value, via the
two devices, after data is applied to the data line;
        maintaining the tie to the clock line by the device to
which the data is sent while the device has not read the data;
and
        maintaining the data on the data line by the device
sending the data at least until the clock line is released by the
device to which the data is sent.

33.   (Previously presented) A method according to Claim
32, wherein one of the two devices is a master device and the
other is a slave device, the master device tying the clock line
to the second logic value before the slave device when data is
transmitted, regardless of the direction in which the data is

transmitted.

34.   (Previously presented) A method according to Claim
33, wherein the master device ties the clock line to the second
logic value after applying data to the data line when the master
device is sending the data to the slave device.

35.   (Previously presented) A method according to Claim
34, wherein the slave device detects the second logic value on
the clock line, then ties the clock line to the second logic
value and reads the data, when the slave device is receiving the
data from the master device.

36.   (Previously presented) A method according to Claim
35, wherein a time period that the slave device has to release
the clock line after receiving data, is independent of any action
by the master device, as the master device does not send any new
data while the slave device has not released the clock line.

37.   (Previously presented) A method according to Claim
33, wherein the master device ties the clock line to the second
logic value when the master receives data from the slave device.

38.   (Previously presented) A method according to Claim
37, wherein the slave device detects the second logic value on
the clock line, then ties the clock line to the second logic
value, and applies the data to the data line, when the slave
device is sending data to the master device.

39.   (Previously presented) A method according to Claim
38, wherein a time period that the slave device has to release
the clock line after sending the data, is independent of any
action by the master device, as the master device does not tie
the clock line to the second logic value to request a new data
until the slave device has released the clock line.

40.   (Previously presented) A method according to Claim
33, wherein when the clock line has the first logic value, a time
period that the master device has to tie the clock line to the
second logic value is independent of any action by the slave
device.

41.   (Previously presented) A method according to Claim
33, further comprising providing the slave device with a
communication interface circuit including:
        a trigger circuit for automatically tying the clock
line to the second logic value when the clock line is changing
from the first logic value to the second logic value;
        an input for applying a clock line release signal to
the trigger circuit; and
        an output for delivering a status signal that has a
first value when the clock line is tied to the second logic value
by the trigger circuit and a second value when the clock line is
released by the trigger circuit.

42.   (Previously presented) A method according to Claim

41, wherein the communication interface circuit further comprises:

a buffer for storing at least one data; and

a circuit for automatically applying the at least one stored data to the data line when the clock line changes from the first logic value to the second logic value.

43.   (Previously presented) A method according to Claim 32, wherein the first logic value is 1 and the second logic value is 0.

44.   (Currently Amended) A data transmitting/ receiving device comprising:

a clock line connection terminal for connection to a clock line;

at least one data line connection terminal for connection to a data line;

a circuit ~~means~~ for tying the clock line to a potential representing a second logic value that is the opposite of a first logic value; and

a data sending unit ~~means~~ for waiting for the clock line to have the first logic value, applying data to the data line, tying the clock line to the second logic value after the data is applied to the data line, then releasing the clock line, and maintaining the data on the data line at least until the clock line has the first logic value, when the data is to be sent.

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45.   (Currently Amended) A device according to Claim
44, further comprising a data receiving unit ~~means~~ for waiting
for the clock line to have the first logic value, tying the clock
line to the second logic value, reading data on the data line,
then releasing the clock line, when the data is to be received.

46.   (Currently Amended) A data transmitting/ receiving
device comprising:
    a clock line connection terminal for connection to a
clock line, the clock line being maintained by default on first
logic value;
    at least one data line connection terminal for
connection to a data line;
    a circuit ~~means~~ for tying the clock line to a potential
representing a second logic value that is the opposite of a first
logic value; and
    a detector ~~means~~ for detecting a change from the first
logic value to the second logic value on the clock line, tying
the clock line to the second logic value, and
            reading the data on the data line, and
        releasing the clock line if data is to be received, or
            applying data to the data line, and releasing
the clock line if data is to be sent.

Claim 47 (Cancelled).

48.   (Currently Amended) A synchronous data
transmission system comprising:

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a clock line;

a data line;

a master data transmitting/receiving device comprising

a clock line connection terminal connected to the
clock line,

at least one data line connection terminal
connected to the data line,

a circuit ~~means~~ for tying the clock line to a
potential representing a second logic value that is the
opposite of a first logic value, and

a data sending unit ~~means~~ for waiting for the
clock line to have the first logic value, applying data
to the data line, tying the clock line to the second
logic value after the data is applied to the data line,
then releasing the clock line, and maintaining the data
on the data line at least until the clock line has the
first logic value, when the data is to be sent; and

a slave data transmitting/receiving device comprising

a clock line connection terminal connected to the
clock line;

at least one data line connection terminal
connected to the data line;

a circuit ~~means~~ for tying the clock line to the
potential representing the second logic value; and

a detector ~~means~~ for detecting a change from the
first logic value to the second logic value on the
clock line, tying the clock line to the second logic
value, reading the data on the data line, and releasing

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the clock line, when the data is to be received.

49.   (Currently Amended) A system according to Claim
48, wherein the master device further comprises a data receiving
unit ~~means~~ for waiting for the clock line to have the first logic
value, tying the clock line to the second logic value, reading
the data on the data line, then releasing the clock line, when
the data is to be received by the master device.

50.   (Currently Amended) A system according to Claim
48, wherein the slave device further comprises a detector ~~means~~
for detecting a change from the first logic value to the second
logic value on the clock line, tying the clock line the second
logic value, applying the data to the data line, and releasing
the clock line, when the data is to be sent from the slave
device.

51.   (Currently Amended) A communication interface
circuit for connection to a data transmitting/receiving device
via a clock line and at least one data line, the circuit
comprising:
        a circuit ~~means~~ for tying the clock line to a potential
representing a second logic value that is the opposite of a first
logic value after data is applied to the at least one data line;
        a trigger ~~means~~ for automatically tying the clock line
to the second logic value when the clock line is changing from
the first logic value to the second logic value;
        an input to apply a clock line release signal to the

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trigger ~~means~~; and

an output to deliver an information signal that has a first value when the clock line is tied to the second logic signal by the trigger ~~means~~ and a second value when the clock line is released by the trigger ~~means~~.

52. (Currently Amended) A communication interface circuit according to Claim 51 further comprising:

storage ~~means~~ for storing data; and

an applicator ~~means~~ for automatically applying the data to the data line when the clock line changes from the first logic value to the second logic value.